Figure 1 is a cross sectional view through a portion of a two interconnected active devices 1, 2 in an integrated circuit. Only a portion of two active devices are shown in Figure 1 since this invention is concerned with techniques for camouflaging the interconnections rather than with the structure of the devices *per se*. The depicted portion of active device 1 is a N-type region 11 that could provide the drain, for example, of a first FET transistor 1 and could be formed as an implanted region with a N-type dopant by techniques very well known in the art. Those skilled in the art will recognize, of course, that the N-type region 11 could alternatively form a portion of a diode, a portion of a bipolar transistor or a portion of some other semiconductor structure. The depicted portion of active device 2 is a N-type region 12 that could form the source, for example, of a second FET transistor 2. The function or functions attributed to regions 11 and 12 are not particularly important to the present invention and they could represent any implanted semiconductor structure as a matter of design choice.

[Please amend the paragraph spanning pages 4 and 5 to read as follows:]

A complicated integrated circuit can literally comprise millions of active regions. Of course, not all active regions or devices are connected to an immediately adjacent active region or device although that is not infrequently the case. With respect to Figure 1, it is assumed that active region 11 and active region 12 require, due to the design of the integrated circuit device in which they are used, interconnection. In the prior art, they might well have been interconnected by providing a thin layer of gold, aluminum or other metallic conductor on the presently exposed surface 15 between implanted regions 11 and 12. However, according to the present invention, regions 11 and 12 are interconnected by a N-type implanted region 13 which provides a conduction channel that interconnects the two active regions 11, 12. In order to camouflage the N-type implant 13, an implant of opposite conductivity type, for example, an implant of P-type conductivity is implanted in a shallower region 14 immediately above the conductive channel formed by region 13.

Please amend the first full paragraph on page 5 to read as follows:

Those skilled in the art will realize that, if the P-type implant 14 were not employed, the N-type implant 13, which has a tendency to extend towards the surface 15 of the semiconductor device shown in Figure 1, might be discoverable by stain and etch techniques. Depending on the type of implantation used, the concentration of the N-type dopant could be higher in regions below surface 15 compared to regions immediately adjacent surface 15. The relatively deeper N-type implant 13 provides a conduction path and will most likely have a relatively high dose of dopant to form the implant (for example, the amount of dosage of the dopant in the conduction path implant 13 could be the same as the dosage used to implant the active regions 11 and 12). The camouflaging implant, namely implant 14, is also a relatively heavy implant, in order to camouflage the opposite conductivity type material in region 13 forming the conducting channel. However, the camouflaging implant 14 is relatively shallow compared to the depth of the conducting implant 13.

B2

Please amend the paragraph spanning pages 6 and 7 to read as follows:

The configurations shown in Figures 1 and 3 will be repeated over and over again on a semiconductor chip, possibly more than a million times depending upon the complexity of the chip. Indeed, the camouflaging implant 14, 24 may be used over essentially 100% of the area of the chip dedicated for use as interconnections and where interconnections between active regions could plausibly occur, but do not occur. As such, said camouflaging implant 14, 24 preferably has a larger area, when viewed in a direction normal to a major surface of the integrated circuit or device, than the area of the conductive channels camouflaged thereby. If the reverse engineer can not infer the presence of a conductive channel merely by the presence of the camouflaging implant 14, 24, it makes the reverse engineer have to work all that much harder to try to determine just how the active regions in an integrated circuit are interconnected. Given the fact that there can be millions of interconnections and even more places where an interconnection could exist (but

B3

B3 Cont.

does not due to the particular requirements of the circuitry on the integrated circuit chip), this invention makes it impracticable for the reverse engineer to try to work out just where the interconnections do exist.

Please amend the paragraph spanning pages 8 and 9 to read as follows:

B4

Figure 5 is a plan view of a small portion of an IC. Four FET transistors T1 - T4 are depicted together with the drains D1 - D4, sources S1 - S4 and gates G1 - G4. Drain D3 and source S4 are depicted as being interconnected by a buried implant 13-1. Drain D4 and source S2 are depicted as being interconnected by a buried implant 13-2. The regions in which interconnections could plausibly occur, but do not occur, and the regions overlying buried interconnects 13-1 and 13-2 are all covered with a camouflaging implant 14, 24. As previously indicated, camouflaging implant 14, 24 is preferably implanted during a single implant process and is only given different numerals herein to differentiate when it overlies an interconnect (labeled numeral 14) and when it overlies regions where interconnections could plausibly occur, but do not occur (labeled numeral 24). The regions where buried interconnection 13 do or do not occur are governed by the particular function or functions to be performed by the IC in question. In the embodiment of Figure 5 it is clear that the camouflaging implant 14, 24 has a significantly larger area, when viewed in a direction normal to a major surface 15 (See Figures 1 & 3) of the IC, than the area of the conductive channels 13-1 and 13-2 camouflaged thereby.